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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/172,553	10/14/1998	JAMES E. GREEN	2914.IUS	9441

7590 06/30/2005

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EXAMINER	
DIAZ, JOSE R	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Response to Rule 312 Communication	Application No.	Applicant(s)	
	09/172,553	GREEN ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *25 May 2005* under 37 CFR 1.312 has been considered, and has been:

   a) ☐ entered.

   b) ☒ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

IN THE CLAIMS:

Claims 1 through 30 and 36 were previously cancelled. Claims 35 and 42 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1.-30. (Cancelled)

31. (Previously presented) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses; and
a plurality of mesas comprising a plurality of contiguous top surfaces, the mesas forming a maze-like structure.

32. (Previously presented) The storage poly of claim 31, wherein the mesas extend in the X, Y and Z coordinates.

33. (Previously presented) A semiconductor capacitor storage poly, comprising:
downwardly extending recesses;
a plurality of webs comprising a plurality of contiguous top surfaces, the webs forming a maze-like structure; and
hemispherical-grain polysilicon on at least some of the plurality of contiguous top surfaces.

34. (Previously presented) The storage poly of claim 33, wherein the webs extend in the X, Y and Z coordinates.

IN THE SPECIFICATION:

Please insert a new paragraph and section heading directly preceding the first paragraph and section heading on page 3 as follows:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of application Serial No. 08/833,974, filed April 11, 1997, now U.S. Patent 6,066,539 issued May 23, 2000.

Please amend the paragraph bridging pages 2 and 3 as follows:

Higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. The advantages of increased miniaturization of components include: ~~reduced bulk~~ reduced-bulk electronic equipment, improved reliability by reducing the number of solder or plug connections, lower assembly and packaging costs, and improved circuit performance. In pursuit of increased miniaturization, DRAM chips have been continually redesigned to achieved ever-higher degrees of integration which has reduced the size of the DRAM. However, as the dimensions of the DRAM are reduced, the occupied area of each unit memory cell of the DRAM must be reduced. This reduction in occupied area necessarily results in a reduction of the dimensions of the capacitor, which, in turn, makes it difficult to ensure required storage capacitance for transmitting a desired signal without malfunction. However, the ability to densely pack the unit memory cells while maintaining required capacitance levels is a crucial requirement of semiconductor manufacturing technologies if future generations of DRAM devices are to be successfully manufactured.

Please amend the third full paragraph on page 6 as follows:

FIG. 23 is an illustration of a scanning electron micrograph of a side ~~cross-sectional~~ cross-sectional view of a storage poly after etching in the formation of a capacitor according to the present invention;